Hindawi Publishing Corporation
Advances in Condensed Matter Physics
Volume 2014, Article ID 632785, 7 pages
http://dx.doi.org/10.1155/2014/632785

Research Article

Fowler-Nordheim Tunneling Characterization on Poly1-Poly2 Capacitors for the Implementation of Analog Memories in CMOS 0.5 μm Technology

Enrique J. Tinajero-Perez,[1] Jesus Ezequiel Molinar-Solis,[1] Rodolfo Z. Garcia-Lozano,[1] Pedro Rosales-Quintero,[2] Jose M. Rocha-Perez,[2] Alejandro Diaz-Sanchez,[2] and Arturo Morales-Acevedo[3]

[1] *Centro Universitario Ecatepec, Universidad Autónoma del Estado de México (UAEMex), Laboratorio de Electrónica, José Revueltas 17, Tierra Blanca, 55020 Ecatepec, MEX, Mexico*
[2] *Instituto Nacional de Astrofísica, Óptica y Electrónica INAOE, Luis Enrique Erro 1, 72840 Tonantzintla, PUE, Mexico*
[3] *Centro de Investigación y Estudios Avanzados del I.P.N, Sección de Electrónica del Estado Sólido, Avenida Instituto Politécnico Nacional No. 2508, Col. San Pedro Zacatenco, 07360 Mexico, DF, Mexico*

Correspondence should be addressed to Jesus Ezequiel Molinar-Solis; molinar@gmail.com

Received 28 October 2013; Accepted 7 January 2014; Published 23 February 2014

Academic Editor: Rodrigo Picos

The experimental results of the Fowler-Nordheim characterization using poly1-poly2 capacitors on CMOS ON Semi 0.5 μm technology are presented. This characterization allows the development, design, and characterization of a new current-mode analog nonvolatile memory. Experimental results of the memory cell architecture are presented and demonstrate the usefulness of the proposed architecture.

1. Introduction

For decades, the floating gate MOS transistors (FG-MOS) have been used as an important element for analog and digital circuit design. Over the years, a wide spectrum of floating gate devices has been proposed for analog applications. Some of them are related to the development of analog nonvolatile memories [1], where the storage of charge in a floating gate (FG) cell is later used as information in voltage-mode or current-mode. This kind of devices is very useful for trimming in analog circuits and information storage for artificial neural networks. Several methods have been used for injecting or removing charge onto a floating gate: the hot electron injection (HEI), Fowler-Nordheim tunneling (F-N) [2], and UV conductances [3]. Over the time, many analog nonvolatile cells have been proposed; Fujita and Amemiya [4] present a structure that has two floating gates connected through a high resistance ~1 GΩ. Though it is a compact cell, it is not achievable in standard CMOS processes, since the integration of such high resistances is not possible.

In the paper [5], Harrison et al. present an on-chip nonvolatile analog memory array. The design uses NMOS transistors with N-well layer as drain in order to address high voltages on chip. Thus, this high voltage is used to allow F-N for programming a specific cell in the whole array. However, the design of an NMOS with this feature violates a design rule related to "active to well edge" in standard CMOS technology.

Figueroa Toro [6] proposes a negative feedback floating gate configuration with two transistors, one capacitor and one inverter amplifier. In this case it is necessary to include an on-chip charge pump, which is used to induce the F-N mechanism. Hence, the design area is augmented by the need of special circuitry.

Moreover, Diorio et al. [7] presents a structure with two PMOS transistors. One transistor has a thin gate oxide that tunnels at much lower voltages. The other transistor

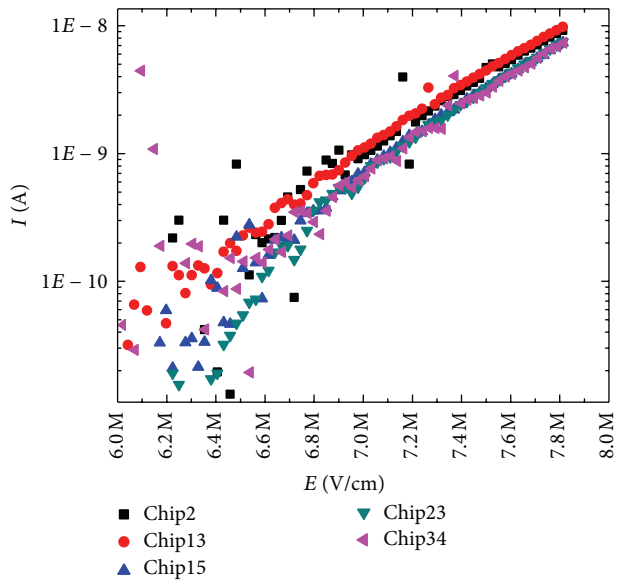

FIGURE 1: Measured tunneling current from five different capacitors I versus E.

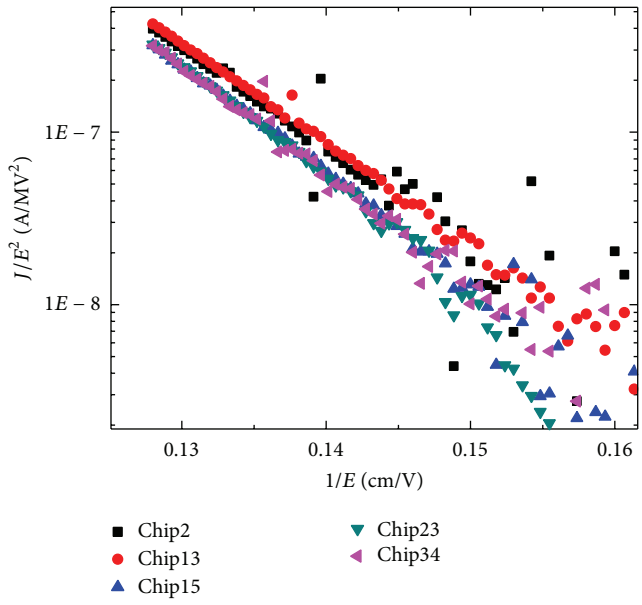

FIGURE 2: F-N plot J/E^2 versus $1/E$.

uses high drain voltages to induce the HEI mechanism in order to increase the electron charge onto the floating gate. Nevertheless, the thin oxide layer tends to degrade with the use of the cell. Thus, the lifetime of the cell is reduced notably.

In this paper, the F-N characterization and the design of a current-mode analog nonvolatile memory are presented. The key element avoids the use of internal high voltages devices (>10 V) on-chip for addressing the F-N programming mechanism. The cell design uses a single floating gate, a poly1-poly2 injector, and a control gate. Thus, F-N tunneling is used to charge and discharge the floating gate. The sections of this paper are organized as follows: the next section will explain the characterization of the F-N current in poly1-poly2 capacitors. Section 3 gives an overview of the cell design. Section 4 reviews the simulations and the experimental results are presented. Finally, the conclusions are presented in Section 5.

2. F-N Characterization on Poly1-Poly2 Capacitors

Depending on the thickness of silicon oxide, there are several electron-transport mechanisms. The F-N tunneling is the dominant mechanism when the oxide thickness is greater than a few tens of nanometers and electrical fields (E_{ox}) greater than 6×10^6 V/cm [2]. The current density (J_{FN}) caused by the F-N tunneling through a SOS (silicon-oxide-silicon) capacitor of area A can be described by the following classical equation:

$$J_{FN} = C_{FN} E_{ox}^2 \exp\left[-\frac{4}{3}\frac{\sqrt{2m_{ox}^*}}{q\hbar}\frac{(q\phi_B)^{3/2}}{E_{ox}}\right], \quad (1)$$

where C_{FN} is a constant, E_{ox} is the electrical field, m_{ox}^* is the effective electron mass in the oxide, q is the electron charge, $\hbar$ is the normalized Planck constant, and ϕ_B is the barrier height between conductor and isolator layer, in this particular case, highly doped polysilicon. As depicted in Figure 1, the I-E_{ox} curves from 5 capacitors fabricated over 5 different chips are shown. When electrical field is less than 6.3 MV/cm, the current is negligible. Moreover, as electrical field increases, electrical current also increases; this suggests that F-N tunneling could be the dominant mechanism. To prove that the transport mechanism is F-N tunneling, it is necessary plot log (J_{FN}/E_{ox}^2) versus $1/E_{ox}$ to obtain a straight line as shown in Figure 2.

The proposed floating gate transistor has a tunneling injector and a control gate (Figure 3). In this device, considering negligible parasitic capacitances, the floating gate potential V_{FG} (potential at FG node with respect to substrate) is approximately given by [8]

$$V_{FG} = \frac{C_1}{C_T}V_C + \frac{C_2}{C_T}V_{tun}, \quad (2)$$

where V_C is the control gate voltage through C_1 capacitor; V_{tun} is the voltage at the charge injector that couples to the floating gate through capacitor C_2, and C_T is the total capacitance of the floating gate.

For this case, the cell is designed with the condition $C_1 \gg C_2$; thus, ratio $C_1/C_T \approx 1$. Hence, floating gate potential V_{FG} is practically defined by control gate potential V_C; that is, $V_{FG} \approx V_C$.

The F-N mechanism allows injecting or extracting electrons from the floating gate. As the potential difference between the floating gate and the charge injector is enough to achieve a critical electrical field, a current is established. The

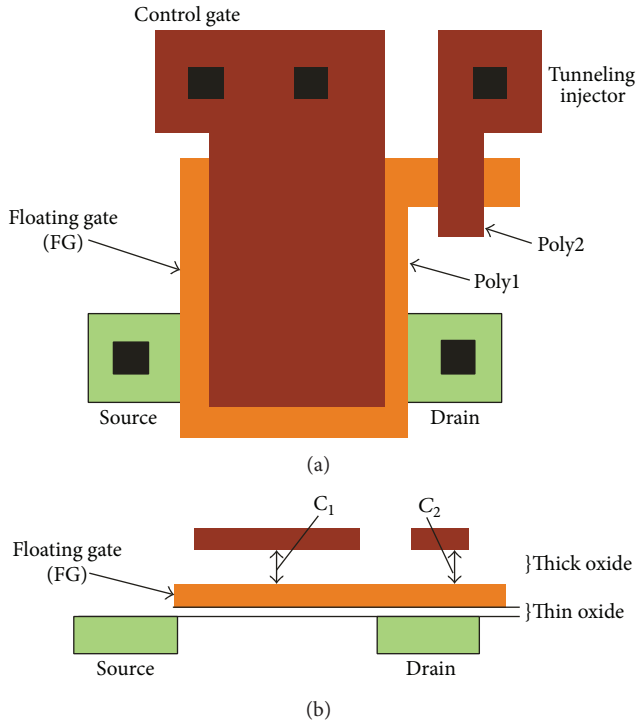

FIGURE 3: Topological design of an FGMOS transistor with a tunneling injector: top view and side view.

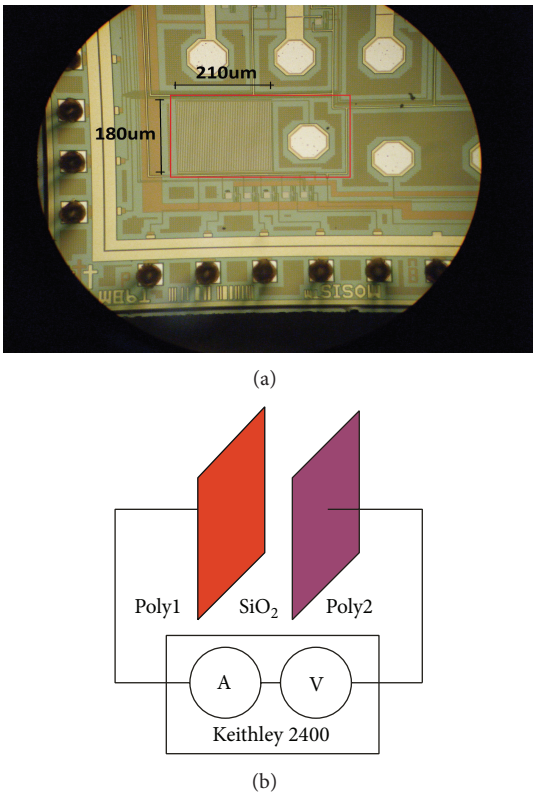

FIGURE 4: (a) Capacitor microphotograph. (b) Measuring equipment and testing structure.

current density is theoretically characterized by the Fowler-Nordheim equation [2]:

$$J = \alpha E^2 \exp\left(-\frac{\beta}{E}\right), \tag{3}$$

where J is the current density, E is the electrical field in the oxide, and α and β are technological constants. For simplicity, we assume that charge injector-floating gate structure is a parallel plate capacitor of area A separated by a distance d. Thus, the electric field in the injector is given by

$$E = \frac{V_{ox}}{d}, \tag{4}$$

where $V_{ox} = V_{tun} - V_{FG}$. Considering that current tunneling is achieved through all the charge injector area, we can express (3) as follows:

$$I_{FN} = A\alpha\left(\frac{V_{ox}}{d}\right)^2 \exp\left(-\frac{\beta d}{V_{ox}}\right), \tag{5}$$

where α and β are fit parameters which must be extracted experimentally from CMOS technology.

In order to obtain α and β from experimental data, (5) must be linearized. Therefore, using natural logarithm in both sides, (5) is transformed to

$$\ln\left(\frac{I_{FN}}{V_{ox}^2}\right) = \ln\left(\frac{A}{d^2}\alpha\right) - \frac{\beta d}{V_{ox}}. \tag{6}$$

This has the linear form

$$y = k - \beta d x, \tag{7}$$

where

$$y = \ln\left(\frac{I_{FN}}{V_{ox}^2}\right), \qquad k = \ln\left(\frac{A}{d^2}\alpha\right), \qquad x = \frac{1}{V_{ox}}. \tag{8}$$

Thus, through the I-V characterization of poly1-poly2 injector, α and β can be extracted using linear fitting.

2.1. Parameter Extraction. Several testing poly1-poly2 capacitors were designed and fabricated on CMOS 0.5 μm technology; these capacitors have an area $A = 180\ \mu\text{m} \times 210\ \mu\text{m}$ and $d = 38.4$ nm (Figure 4). The I-V curves from 40 capacitors were obtained using Keithley 2400 sourcemeters. The extracting methodology was accomplished with the arithmetic average of the I-V curves. The following values for $\alpha = 86.51 \times 10^{-12}\ \text{A/V}^2$ and $\beta = 150.56\ \text{MV/cm}$ were obtained; consequently, the F-N current expression is

$$I_{FN} = 86.51 \times 10^{-12}\left(\frac{\text{A}}{\text{V}^2}\right) A \left(\frac{V_{ox}}{d}\right)^2 \times \exp\left(-\frac{150.56 \times 10^6\ (\text{V/cm})\, d}{V_{ox}}\right). \tag{9}$$

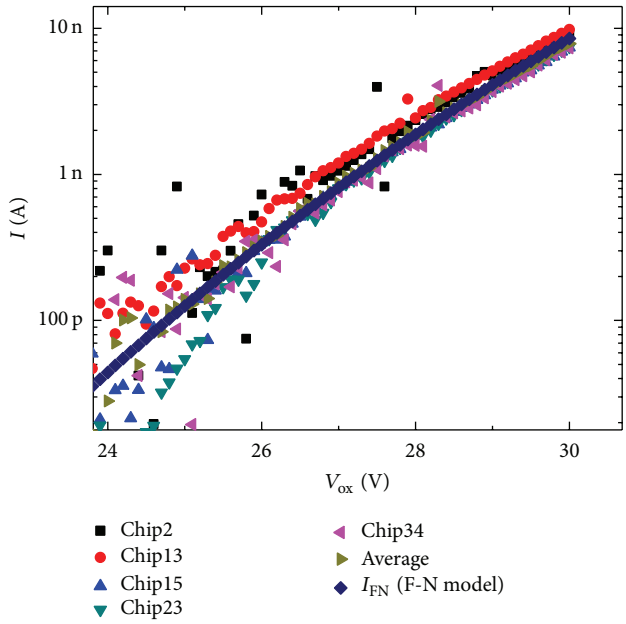

Figure 5: Five structures with F-N tunneling current, average curve, and F-N model using technological parameters.

Table 1: Electrical values for the memory cell.

Electrical parameter	Value
V_{DD1}	3.3 V
V_{DD2}	8 V
C_1	1 pF
C_2	3 fF
C_{par}	360 fF
R_1, R_2	1*E*99 Ω
$MFG_{1,2}$	6 μm/3 μm
*M*1, *M*2, *M*4, *M*5	6 μm/3 μm
*M*3	30 μm/1.5 μm
*M*6, *M*9	12 μm/6 μm
*M*7, *M*8	30 μm/6 μm
*M*10	12 μm/6 μ
*M*11	60 μm/6 μm
*M*12	100 μm/1.5 μm
I_{bias}	50 μA
V_{ref}	1.5 V
V_{b1}	3.3 V
V_{read}	0–3.3 V

This expression brings a close approximation for the F-N current for a given poly1-poly2 tunneling injector with area A and distance d between plates.

Only five *I-V* curves from different capacitors are shown for clarity in Figure 5; the average curve and the I_{FN} model for the capacitors are also shown in the same plot. A good fitting among *I-V* measurements, average, and the proposed I_{FN} model can be noticed.

3. Memory Cell Design

The current-mode analog memory cell proposed in this paper stores charge onto the floating gate of MFG_1 and MFG_2 transistors in order to set a given current I_{mfg} and I_{out}, (Figure 6). This current is stored permanently and results from the copy of an input current I_{in} by using a feedback loop. Thus, the stored charge can be read out as an analogue current from MFG_2. Some important electrical characteristics of the cell are presented in Table 1.

The operation of the storage cell is explained in three stages as follows.

3.1. Initialization. The capacitor C_2 is set to an initial potential of $V_{tun} = -25$ V and transistor M12 must be turned on in order to lead V_c to ground. This condition $V_c = 0$ V sets $V_{FG} = 0$ V through capacitor C_1. As a result, $V_{ox} = -25$ V enabling F-N tunneling current through poly1-poly2 capacitor C_2. Consequently, electrons are injected to the FG causing a potential drop of V_{FG} relative to ground, increasing the current I_{mfg} from MFG_1 transistor. This memory has been verified to store analogue current values in the range of 30 μA $< I_{out} <$ 70 μA; therefore, the initial current condition must fulfill $I_{mfg} > 70$ μA for a proper operation of the cell feedback loop.

3.2. Programming. The programming stage starts setting an input current value I_{in}, which will be stored in the cell permanently. A potential of $V_{tun} = 25$ V must be also established on C_2 and transistor M12 must be turned off. The current to be stored is introduced by the current source I_{in}, where transistors M1, M2, and M3 act as a cascode current mirror with high output impedance at node "x." Thus, node "x" will have high gain and since $I_{mfg} > I_{in}$, the potential in this node will be close to V_{DD1}. The comparator allows even a higher gain from node "x" and was considered in order to reduce the error of I_{out}/I_{in}. Moreover, this comparator allows an adjustable reference through V_{ref}. The push-pull inverter brings a rail-to-rail output from the comparator output; indeed, this inverter has a $V_{DD2} = 8$ V whose output V_c is induced to the FG through capacitor C_1.

Thus, when voltage at node "x" is close to V_{DD1}, the inverter brings $V_c = 0$ V which sets the FG also to 0 V, as mentioned above. This voltage difference between V_{tun} and V_{FG} is greater than 24 V ($V_{ox} > 24$ V); then, electron tunneling is achieved, which extracts electrons from the FG causing an increase on V_{FG}. As a result, the current I_{mfg} is decreased. Consequently, potential V_{FG} rises until node "x" reaches $I_{in} \approx I_{mfg}$ by the use of the feedback loop. When I_{in} is slightly greater than I_{mfg}, the potential at node "x" drops to a value near ground; this causes a "high" output from the inverter, $V_c = 8$ V. This 8 V output of the circuit applied to C_1 capacitor stops tunneling since now $V_{ox} < 24$ V. This control loop makes this cell a novel design since only 8 V on-chip is necessary in order to stop tunneling with the feedback loop.

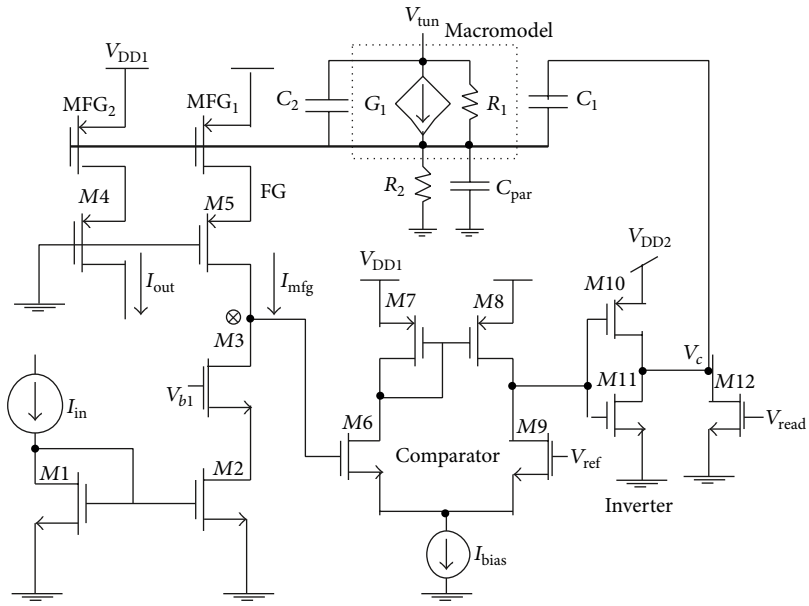

Figure 6: Analog current-mode memory cell.

Finally, I_{mfg} current of MFG transistor will be equal to I_{in} current, which is permanently stored by means of the stored charge in the FG.

3.3. Reading. Cell reading is performed under the following conditions: $V_{tun} = 0\,V$ and $V_c = 0\,V$. For this purpose, transistor M12 must be turned on in order to lead V_c to ground. The output current I_{out} is a copy of I_{mfg} and is obtained from the drain of transistor M4.

4. PSpice Simulations and Experimental Results

4.1. Macromodel for I_{tun} Electrical Simulation. Spice is a world standard program for electrical circuit simulation. A macromodel is a combination of Spice models used for a special purpose device. Since F-N tunneling current is not modeled in Spice, the F-N expression is implemented as a macromodel with the use of a voltage-controlled current source (VCCS); that is,

$$G1\ 1\ 2\ \text{VALUE} = \left\{190.1e-9 * [V(1) - V(2)]^2 * \text{EXP}\left\{\frac{-578.15}{[V(1) - V(2)]}\right\}\right\} \quad (10)$$

$$R1\ 1\ 2\ 1e99,$$

where "G" is associated with a voltage controlled current source and 1 and 2 are the nodes where the current source is connected. Node 1 represents external applied voltage V_{tun} which is ground referenced and node 2 represents the V_{FG}. The "VALUE" parameter allows the implementation of (9) including the injector area of C_2; in this case $A = 1.8\,\mu m \times 1.8\,\mu m$ and distance $d = 38.4\,nm$. Additionally, a resistor R1 is included with a high value in order to improve simulation convergence. The VCCS G1 and R1 are shown in dashed line in Figure 6.

4.2. Spice Electrical Cell Simulation. An electrical cell simulation using PSpice is shown in Figure 7. The cell also includes resistor R2, which is used for improving convergence and helps the simulator to set the DC operation point at the floating gate. Furthermore, capacitor C_{par} models the FG-*substrate* parasitic capacitor. In this case this capacitor can be calculated using the layer capacitance parameters given by the foundry and the injector area, in this case, has a value of $C_{par} = 360\,fF$. When an input current $I_{in} = 70\,\mu A$ is established on the cell, the initial output current is $I_{mfg} = 160\,\mu A$ and after 40 s this output current drops to ~70 μA. At this point, V_C rises to 8 V and F-N tunneling is stopped. Afterwards, at 50 s, the V_{tun} is removed and transistor M14 is turned on; this enables the readout current, $I_{out} = 70.1\,\mu A$. The cell worked properly at the range $70\,\mu A < I_{out} < 30\,\mu A$. The highest error, error = $|I_{out} - I_{in}|$, is obtained when current values are near 30 μA. It is important to notice that although a deviation in (9) could be present, only the cell convergence time to reach $I_{in} \approx I_{mfg}$ would be affected by several seconds. A microphotograph of a chip is shown in Figure 8.

The measured relative error percentages for several programming input current values are shown in Figure 9. The error calculation was considered using

$$\text{error}\,\% = \left|\frac{I_{out} - I_{in}}{I_{in}}\right| \times 100. \quad (11)$$

From experimental data, the error is less than 5% in the range $70\,\mu A < I_{out} < 50\,\mu A$. Therefore this is considered the working range of the cell. In Figure 10, the plot shows a set of five cells supplying currents between $I_{out} = 60\,\mu A$ to $65\,\mu A$

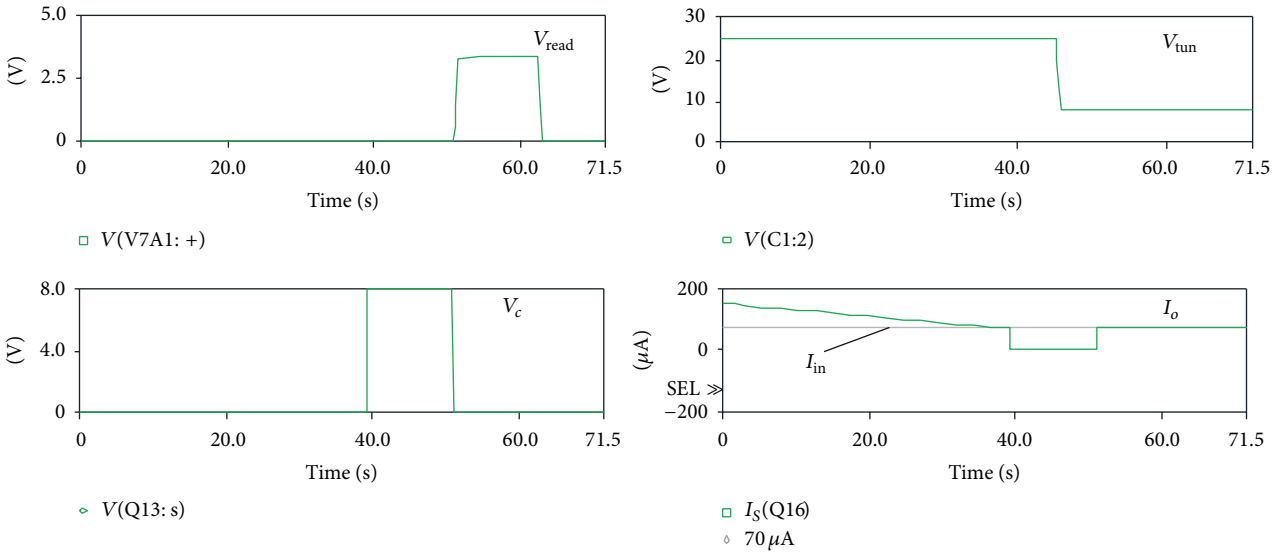

Figure 7: Transient simulation of the analog memory cell for a 70 μA input current.

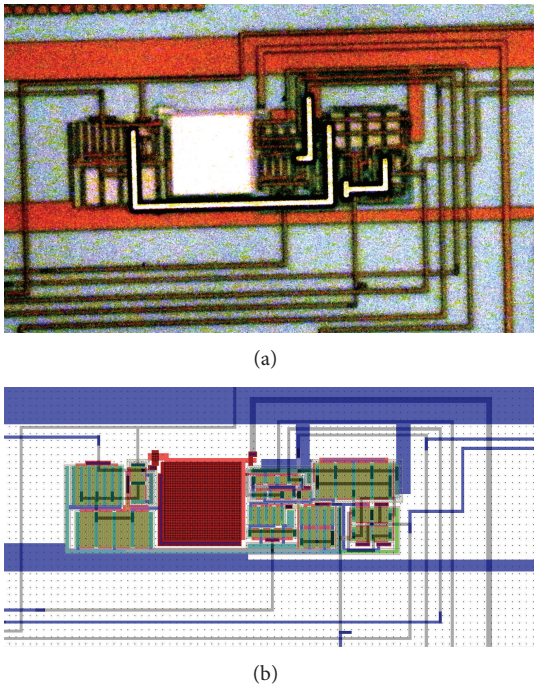

Figure 8: Memory cell microphotograph and layout.

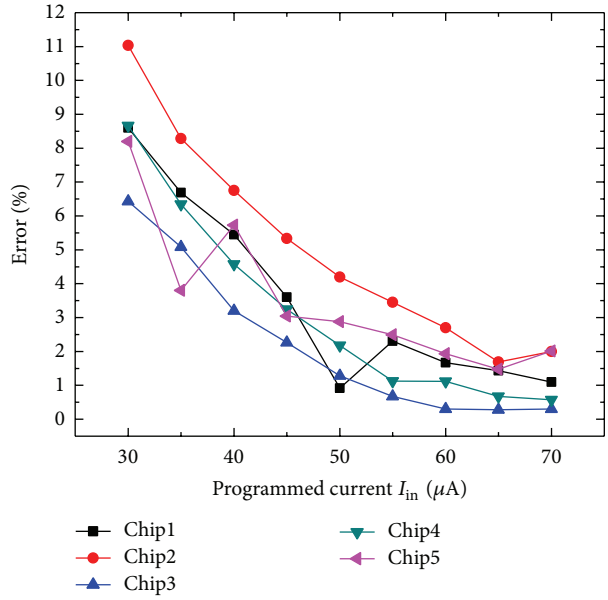

Figure 9: Error percentage from output current I_{out} for several input current values I_{in}.

over a long period of time. The charge retention of the floating gate has been confirmed by the measurements of the cells over 1000 minutes. In submicron technologies, gate leakage is well known [9]; thus, a constant measurement of the cell could show a change in the charge trend. Nevertheless, a further statistical analysis of this situation should be considered for periods $\gg$ 1000 min, since this could give important information about the usefulness of the cell, that is, reliability and refreshing cycles.

In Figure 11, the graph shows ambient temperature measurement at the same time span. A correlational fluctuation of the current value is observed and caused by the ambient temperature. Considering ΔI_{out} from Figure 10 and ΔT from Figure 11, the storage cell presents a temperature dependence of −221 nA/°C. Therefore, the stored charge onto the floating gate does not present a significant change at the same period of time.

5. Conclusions

In this work, a novel nonvolatile current-mode analog memory cell architecture is presented. A control loop is used with only 8V to stop F-N tunneling. This is a new approach that allows the use of standard circuitry internally in order

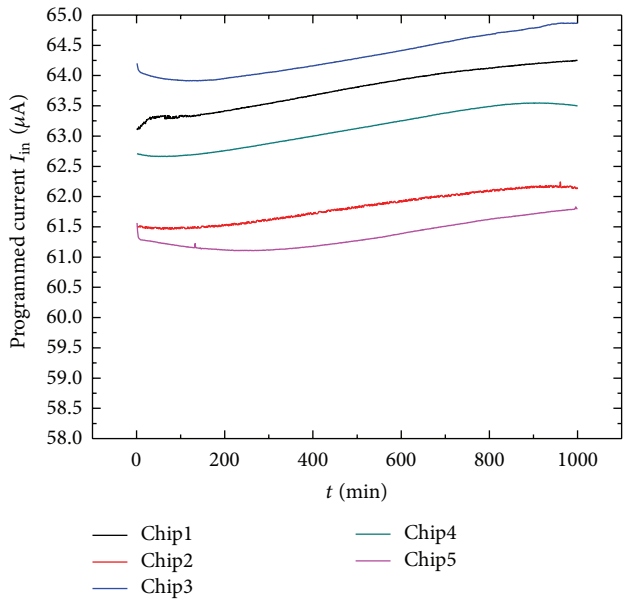

FIGURE 10: Output current I_{out} in a time span of 1000 minutes.

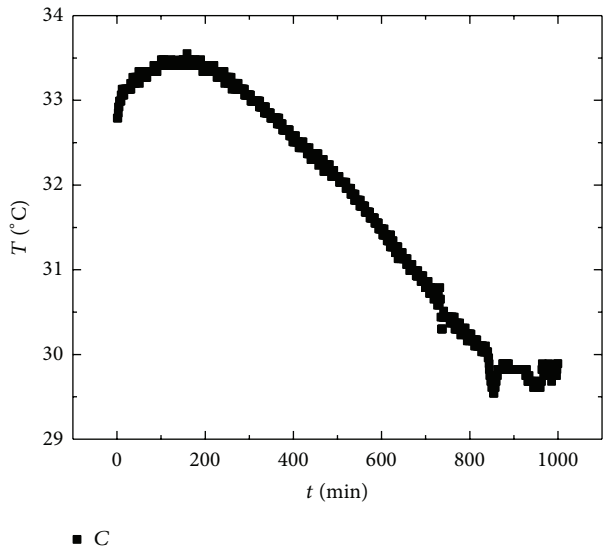

FIGURE 11: Ambient temperature variation.

to program nonvolatile analog cells on chip. Experimental results show that the cell presents a useful range of values with a maximum error of 5%. The functionality of the cell was analyzed through a long period of time (1000 min) and also temperature performance was analyzed.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

[1] B. A. Minch, P. Hasler, and C. Diorio, "Synthesis of multiple-input translinear element networks," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '99)*, vol. 2, Orlando, Fla, USA, June 1999.

[2] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO2," *IEEE Transactions on Electron Devices*, vol. 15, no. 9, 1968.

[3] R. G. Benson and D. A. Kerns, "UV-activated conductances allow for multiple time scale learning," *IEEE Transactions on Neural Networks*, vol. 4, no. 3, pp. 434–440, 1993.

[4] O. Fujita and Y. Amemiya, "Floating-gate analog memory device for neural networks," *IEEE Transactions on Electron Devices*, vol. 40, no. 11, pp. 2029–2035, 1993.

[5] R. R. Harrison, J. A. Bragg, P. Hasler, B. A. Minch, and S. P. Deweerth, "A CMOS programmable analog memory-cell array using floating-gate circuits," *IEEE Transactions on Circuits and Systems II*, vol. 48, no. 1, pp. 4–11, 2001.

[6] M. E. Figueroa Toro, *Adaptive signal processing and correlational learning in mixed-signal VLSI [Ph.D. dissertation]*, University of Washington, 2005.

[7] C. Diorio, D. Hsu, and M. Figueroa, "Adaptive CMOS: from biological inspiration to systems-on-a-chip," *Proceedings of the IEEE*, vol. 90, no. 3, pp. 345–357, 2002.

[8] A. K. Sharma, *Advanced Semiconductor Memories, Architectures, Designs and Applications*, John Wiley & Sons, 1st edition, 2003.

[9] P. Hafliger and H. K. O. Berge, "Exploiting gate leakage in deep-submicrometer CMOS for input offset adaptation," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 2, pp. 127–130, 2007.